IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Craig T. Salling, et al. Art Unit: 2813

Serial No.: TBD Examiner: David L. Hogans

Filed: Herewith Docket: TI-32206.1

For: Method to Increase Substrate Potential in MOS Transistors Used in ESD Protection Circuits

LETTER TO THE OFFICIAL DRAFTSPERSON

"EXPRESS MAILING" Mailing Label No. **EV334469215US**. I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 CFR 1.10 on the date shown below and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Karen Vertz 7-29-03

Karen Vertz Date

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed are **SEVEN (7)** sheets of formal drawings for the above-referenced case. Please charge any necessary fees to Deposit Account No. 20-0668 of Texas Instruments Incorporated. This sheet is enclosed in triplicate.

Respectfully submitted,

Gary C. Honeycutt

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Dallas, Texas 75265

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